

(12) UK Patent Application (19) GB (11) 2 210 531 A (13)

(43) Date of A publication 07.06.1989

(21) Application No 8822827.5

(22) Date of filing 29.09.1988

(30) Priority data

(31) 62 148 529 (32) 29.09.1987 (33) JP

(71) Applicant

Sony Corporation

(Incorporated in Japan)

7-35 Kitashinagawa 6-chome, Shinagawa-ku, Tokyo,
Japan

(72) Inventor

Naoki Nishio

(74) Agent and/or Address for Service

J A Kemp and Co

14 South Square, Gray's Inn, London, WC1R 5EU,
United Kingdom

(51) INT CL^a

H04N 7/087 // H04N 5/18 5/202 5/208

(52) UK CL (Edition J)

H4F FBB FD1B1 FD1D1 FD1K1 FD12X FD22
FD30A3 FD30D2 FD30E FD30G FD30H FD30K
FD30P FD30T1 FGY FHH FHL

(56) Documents cited

BBC Research Department Report, number BBC RD
1986/5, June 1986

(58) Field of search

UK CL (Edition J) H4F FBB FGXX FGY FHH FHL
INT CL^a H04N

(54) Signals inserted into blanking intervals control subsequent processing

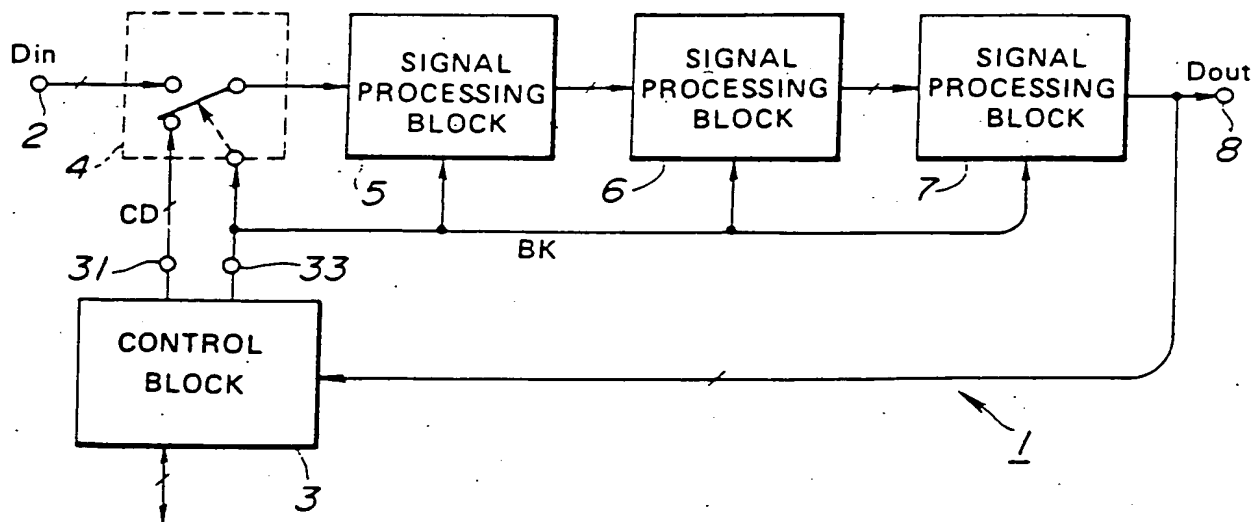
(57) The output signal of a video camera is digitised and applied to the input terminal 2 of a signal processing arrangement comprising several series - connected processing blocks 5, 6, 7, each block providing one processing operation. In the embodiment block 5 provides gamma correction, block 6 aperture correction and block 7 black and white level clip.

Control block 3 inserts operation control data CD into the blanking intervals of the incoming digital video signal.

The operation control data specifies which processing operations are to be performed - each processing block functioning only when its respective control data is present.

Details of the gamma correcting block, the aperture correcting block and the level clipping block are shown in Figs 3-7, 8-10 and 11 to 17 respectively.

FIG. 2



This Page Blank (uspto)

1/9

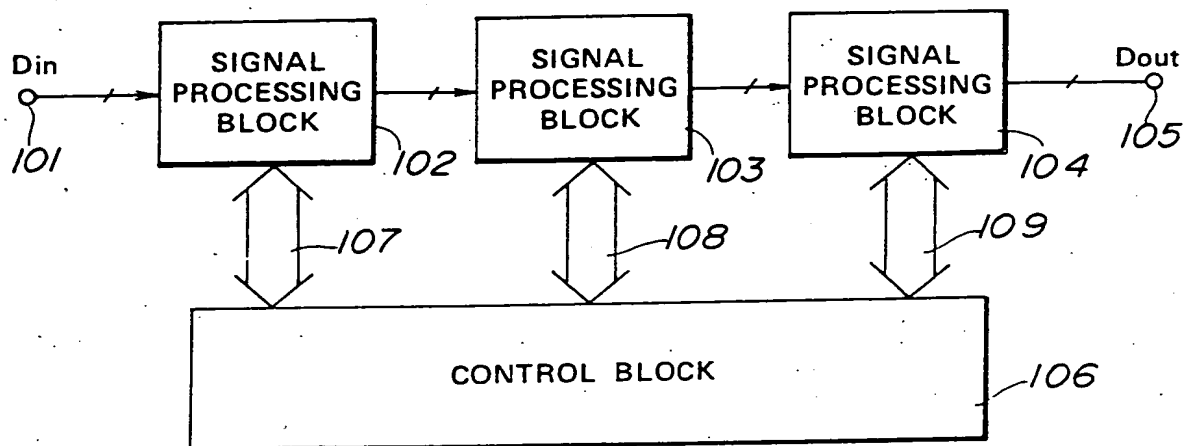
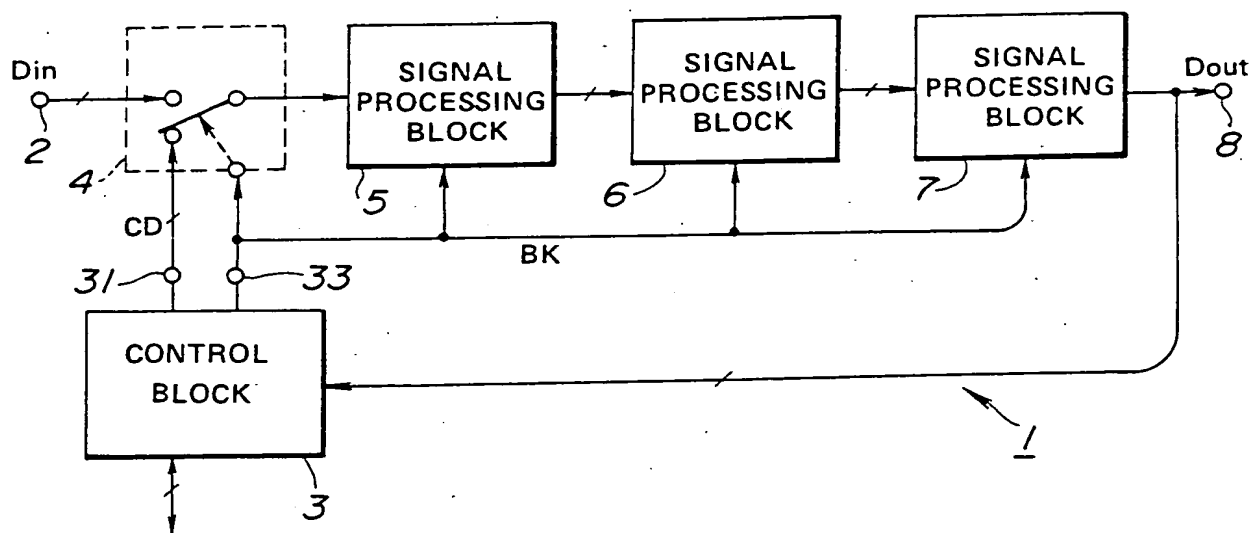
FIG. 1**FIG. 2**

FIG. 3

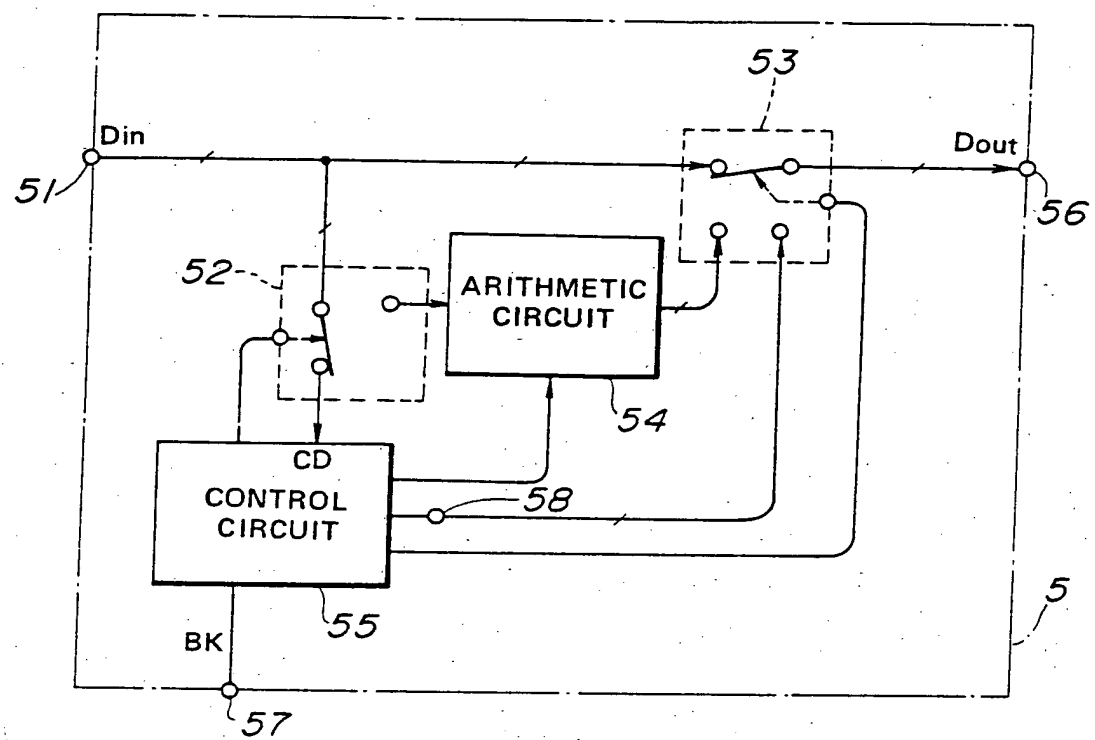


FIG. 4

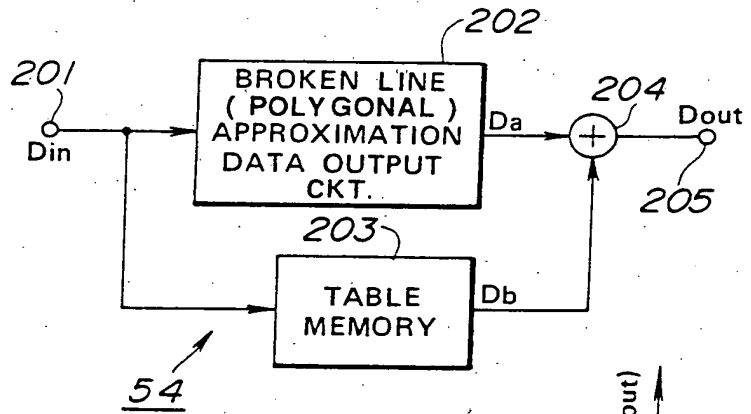
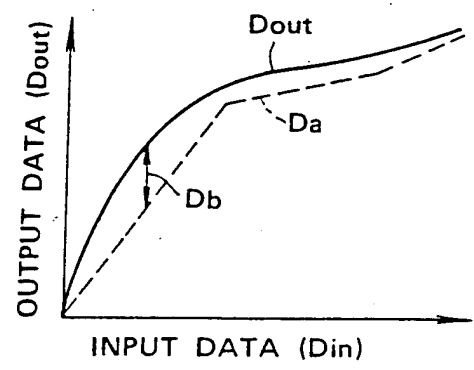
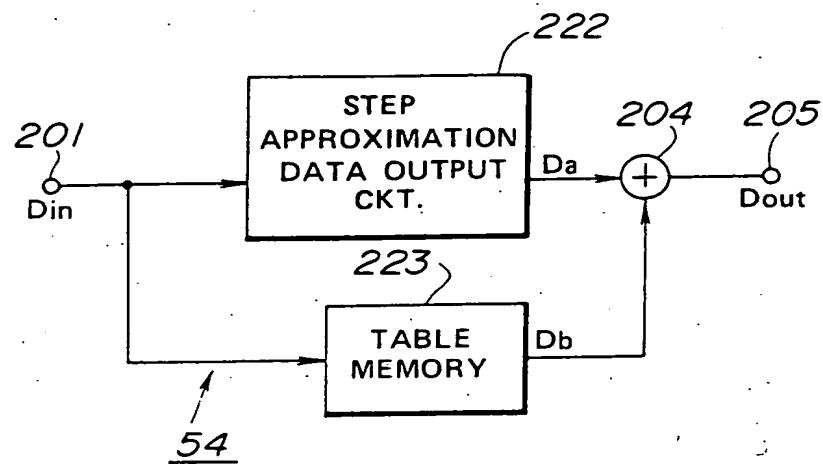
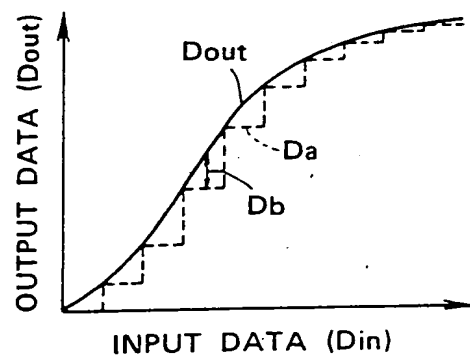


FIG. 5

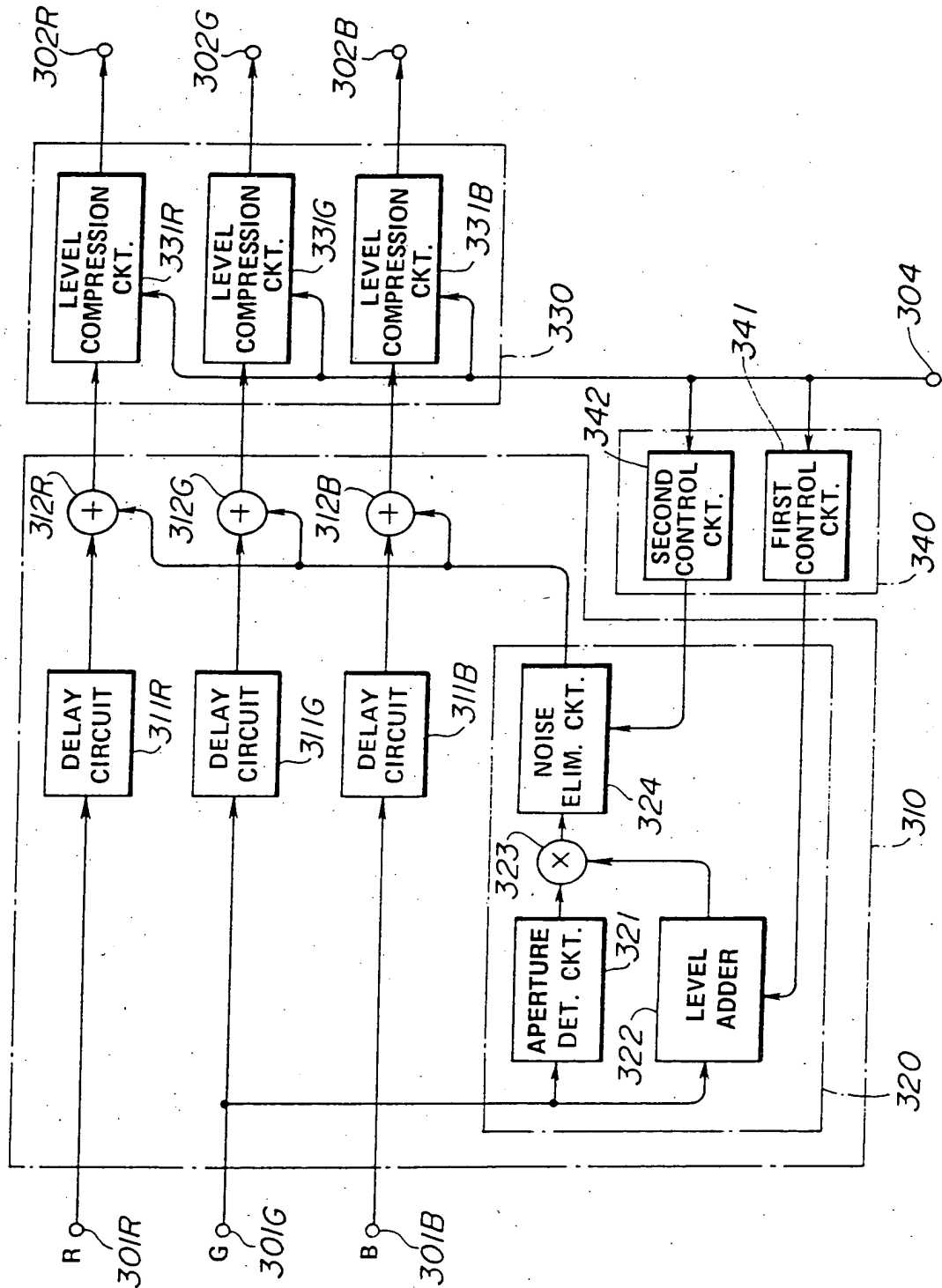


3/9

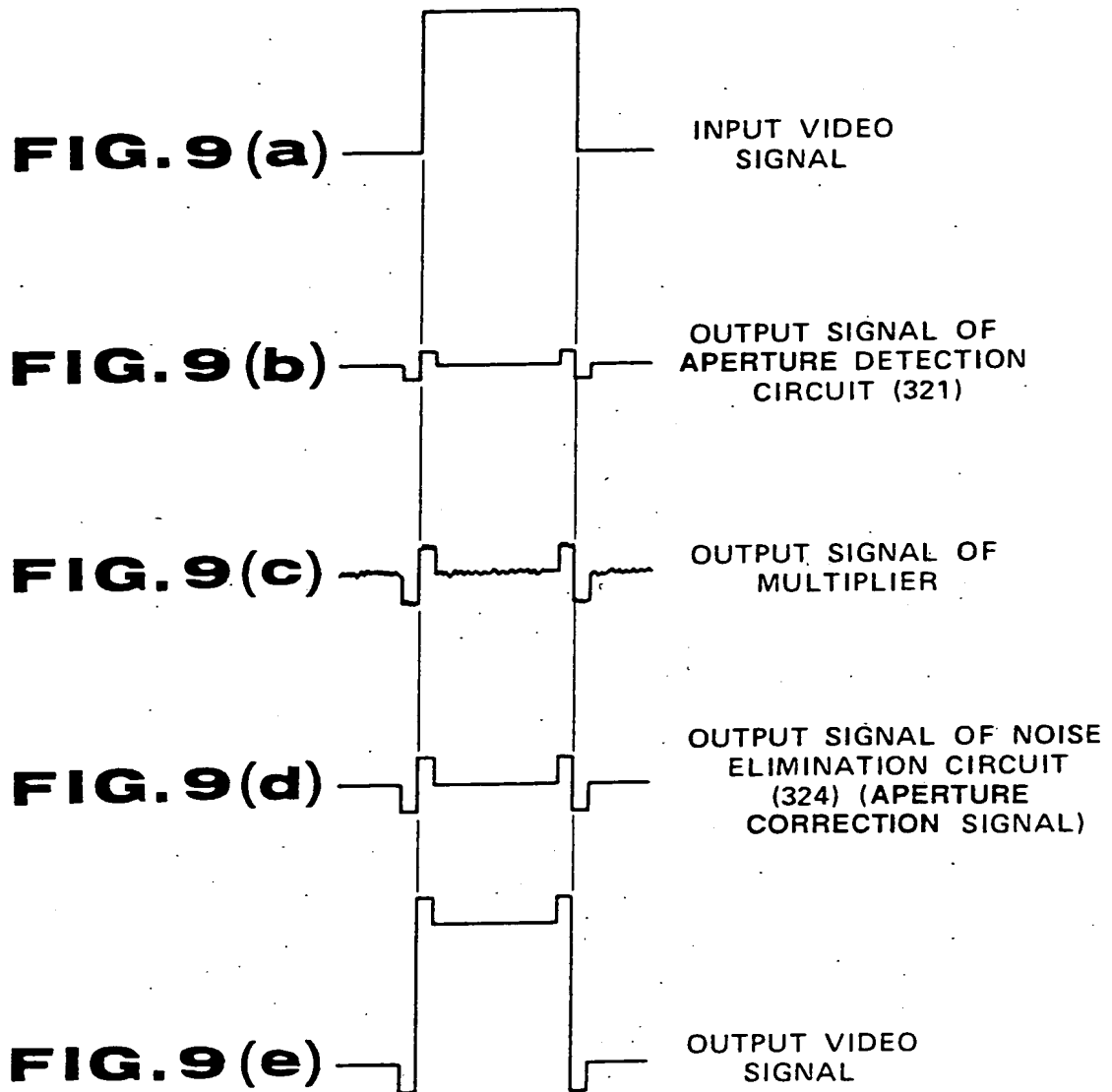
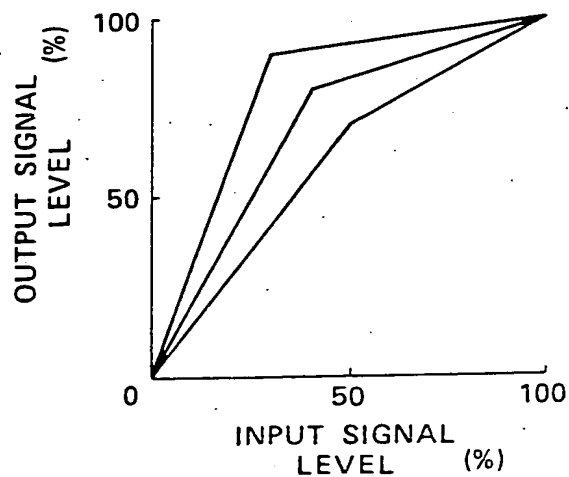
FIG. 6**FIG. 7**

4/9

FIG. 8

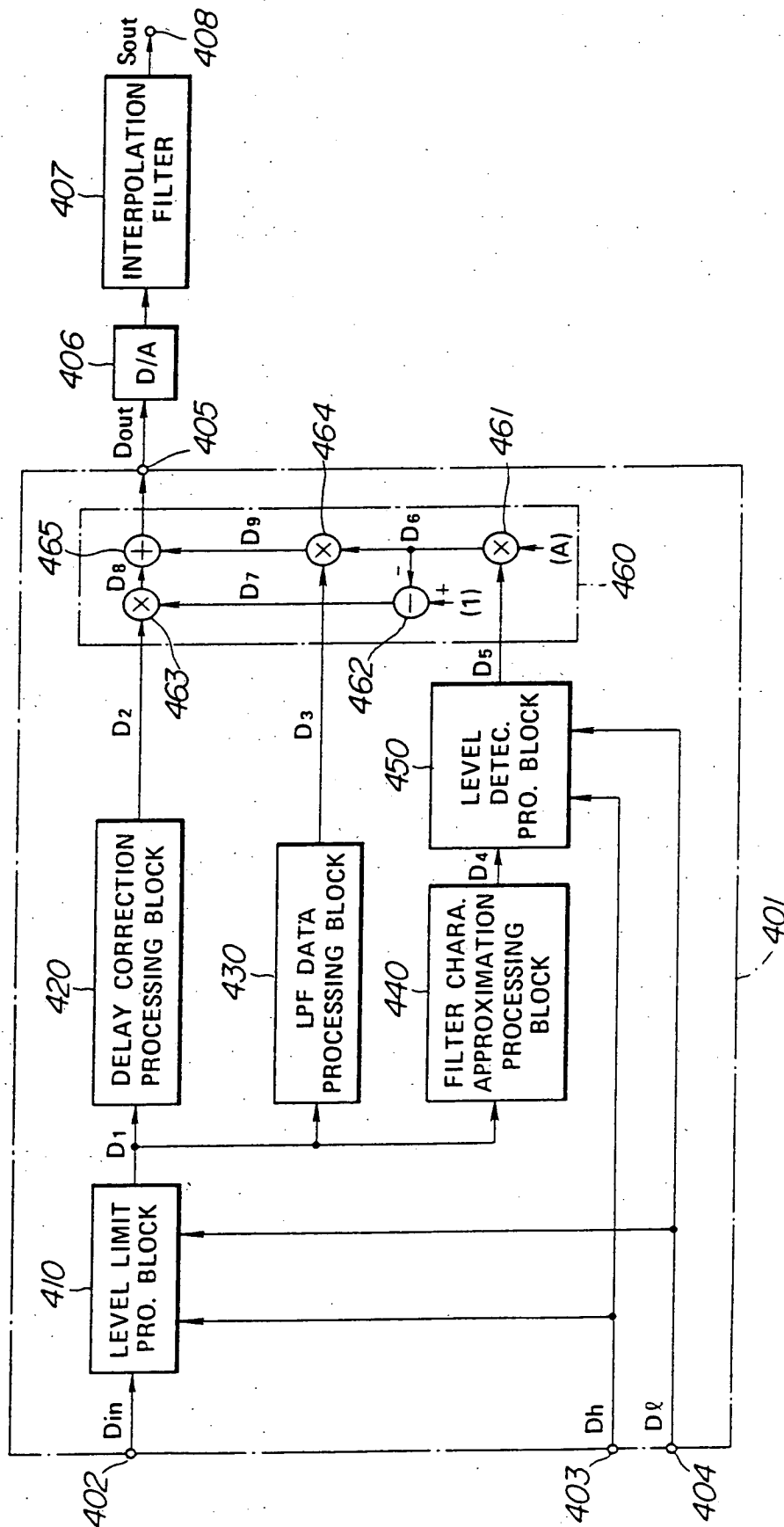


5/9

**FIG. 10**

6/9

FIG.11



7/9

FIG.12(b) FIG.12(d) FIG.12(f)
FIG.12(a) FIG.12(c) FIG.12(e)

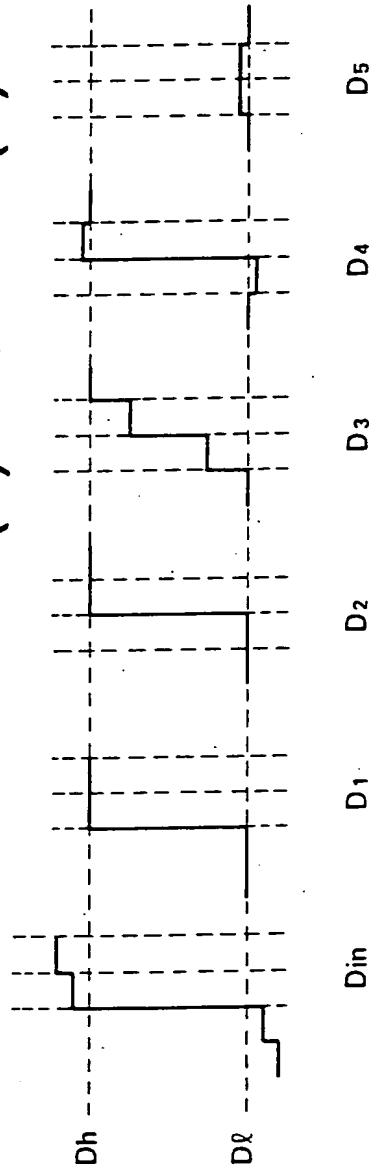
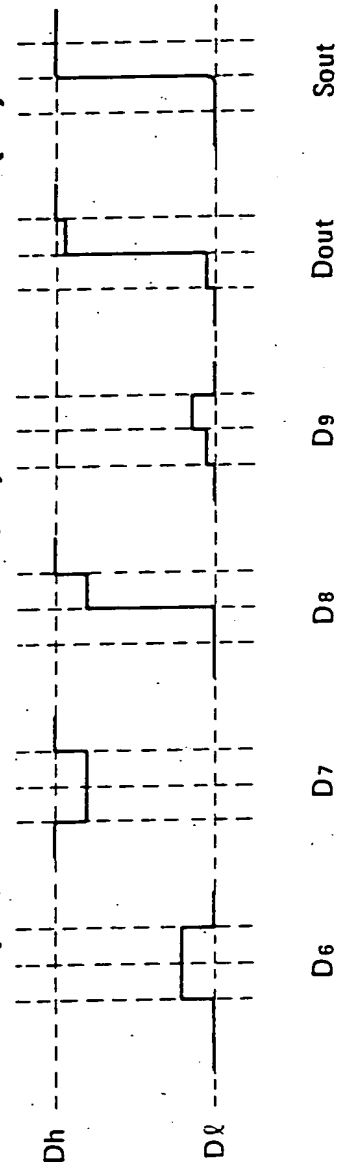
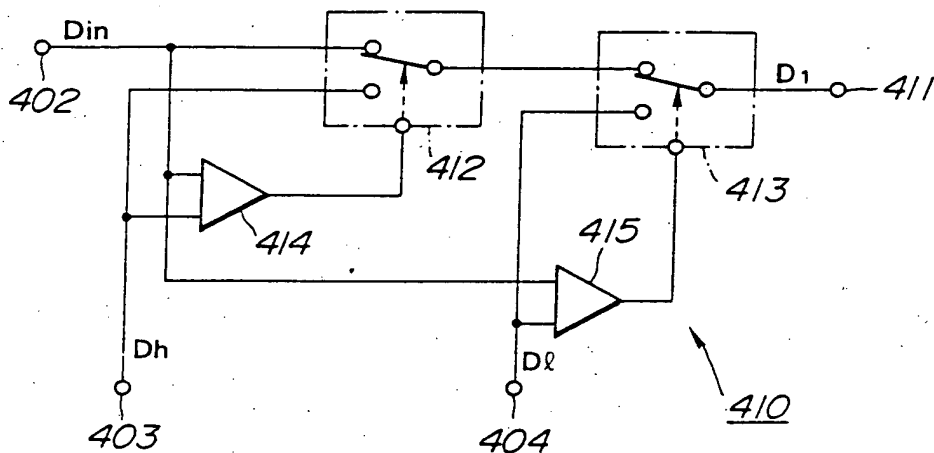
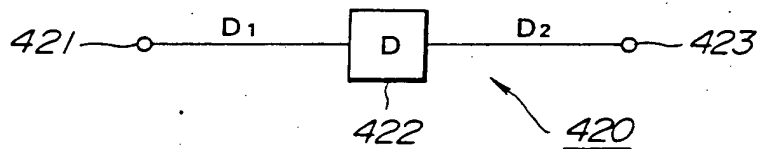
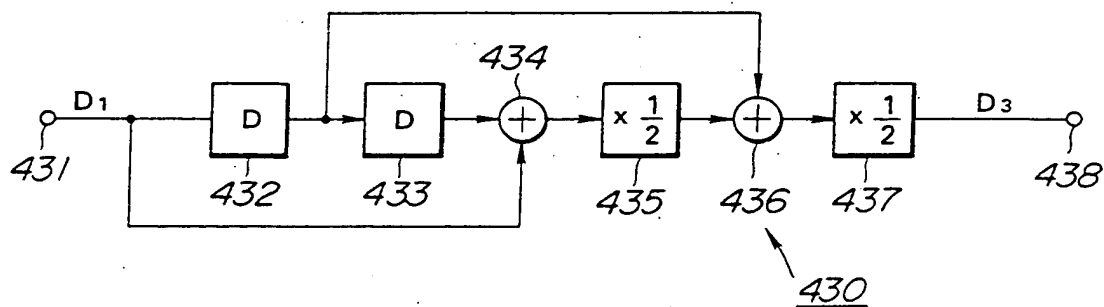


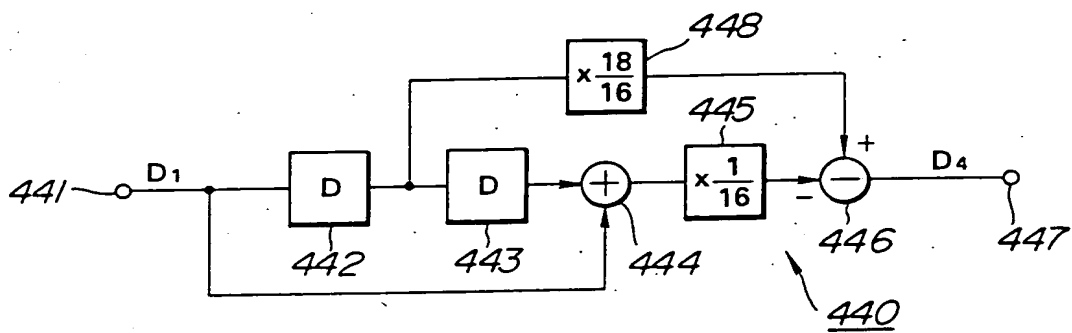
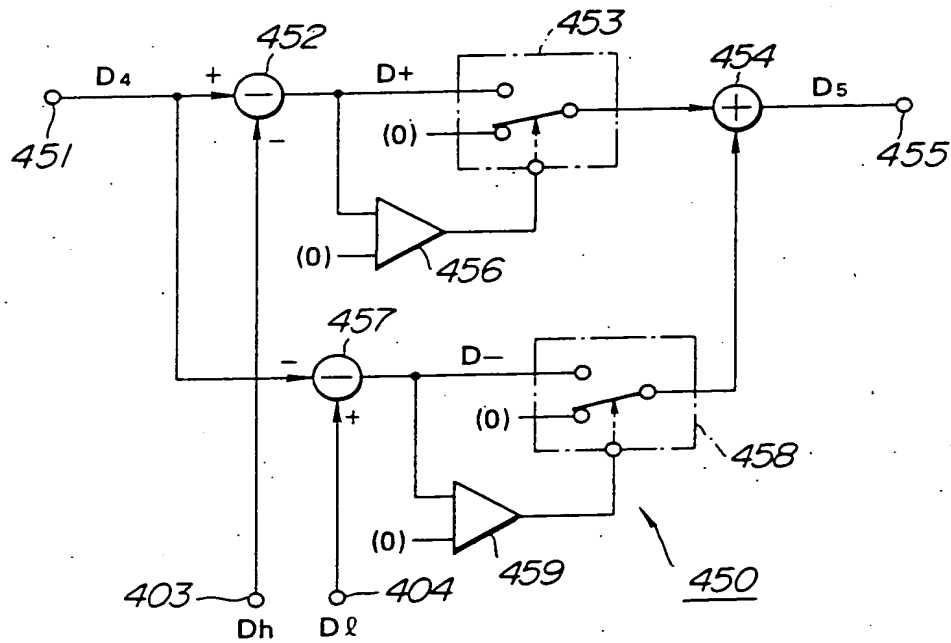
FIG.12(h) FIG.12(j) FIG.12(l)
FIG.12(g) FIG.12(i) FIG.12(k)



8/9

FIG. 13**FIG. 14****FIG. 15**

9/9

FIG. 16**FIG. 17**

This Page Blank (uspto)

A CIRCUIT FOR PROCESSING A DIGITAL SIGNAL HAVING A
BLANKING INTERVAL

BACKGROUND OF THE INVENTION

(1) Field of the Invention

5 The present invention relates to a circuit for
processing a digital signal such as a digital video
signal having a blanking interval. The present invention
relates specifically to the digital processing circuit
in which signal processings in a plurality of signal
10 processing blocks are controlled on the basis of
operation control data added into the blanking interval
of the input digital signal, whereby the circuit
construction can be simplified and the complex signal
processing can be carried out.

15 (2) Background of the Art

Photographing equipment such as a video camera
generally converts an optical image on a surface of a
photographic (image pick-up) element into an electrical
video signal and produces a standard NTSC (National
20 Television System Committee) color television signal
under various signal processings for the video signal
such as a white balance adjustment and gamma correction,
etc..

In addition, in such a photographing equipment
25 the NTSC standard color television signal is provided
with a blanking interval, i.e., a line returning interval
of scanning lines during which no video image is
reproduced. The blanking interval means time intervals
between the video signal effective intervals, i.e.,
30 between the effective signal segments including video
information.

Recently, along with developments of digital
signal processing techniques, a digital signal
processing circuit has been used in a signal processing
35 system of video signals.

For example, as shown in Fig. 1, such a

digital signal processing circuit includes a data input terminal 101 to which an input digital signal is supplied, a plurality of signal processing blocks 102, 103, and 104 for carrying out predetermined signal processings such as a white balance adjustment and gamma correction for the input digital signal D_{in} , and a data output terminal 105, each circuit block and terminal being connected in series with each other.

Furthermore, a control circuit block 106 for controlling each signal processing of the signal processing blocks 102, 103, and 104 is connected to each signal processing block 102, 103, and 104 via respective control signal lines 107, 108, and 109.

In the above-described signal processing circuit, each signal processing block 102, 103, and 104 is formed of an IC (Integrated Circuit). Their operation controls are directly carried out by means of the above-described control block 106 via each control signal line 107, 108, and 109 so that the predetermined signal processings for the input digital signal D_{in} are carried out at the respective signal processing blocks 102, 103, and 104 to output the output digital processed signal D_{out} via the data output terminal 105.

The number of signal lines connected to the respective signal processing blocks 102, 103, 104 formed of such as the above-described ICs, in the video signal processing circuit, are amounted to approximately more than 100 including the signal lines for outputting and inputting data of color components such as red (R), green (G), and blue (B) of the image pick-up signals, the control signal lines 107, 108, and 109, power supply lines and clock signal lines.

However, the digital signal processing circuit formed of integrations of several large-scale ICs has problems of excessive number of signal lines and of very complex circuit construction.

Furthermore, another digital signal processing circuit is demanded which can carry out the more complex signal processings for the input digital signal. Accordingly, such signal processing blocks as being
5 capable of inputting and outputting tremendous amounts of data such as for operation controls are needed. One of methods for inputting and outputting tremendous amounts of data without increase of the signal lines connected to the signal processing blocks includes,
10 e.g., data serial transmission method. However, time errors are generated for the signal processings of the video signals and accordingly a hardware for the reception and transmission of data becomes needed.

Consequently, there is no sufficient method of
15 solving the problems at the present time.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide an improved digital signal processing circuit which can achieve a complicated
20 signal processing with a relatively simple construction.

It is another object of the present invention to provide an improved digital signal processing circuit which can decrease the number of signal lines.

According to one aspect of the present
25 invention there is provided a digital signal processing circuit having a plurality of signal processing circuit blocks and a control block which control the operations of the signal processing blocks. The apparatus comprises combining means for combining an operation control data
30 into a blanking interval of an input digital signal, control block, and cascade connected signal processing blocks in which the input digital signal is processed in accordance with the operation control data read from the input digital signal during the blanking interval.

35 In the digital signal processing circuit according to the present invention, signal lines for

inputting or outputting the input digital signals are utilized for inputting or outputting an operation control data between the signal processing blocks and control block.

5 BREIF DESCRIPTION OF THE PREFERRED EMBODIMENT

Fig. 1 is a simplified circuit block diagram of a previously proposed digital signal processing circuit.

10 Fig. 2 is a simplified circuit block diagram of another digital signal processing circuit in a preferred embodiment according to the present invention.

Fig. 3 is a simplified circuit block diagram of a signal processing block in the preferred embodiment shown in Fig. 2.

15 Fig. 4 is a simplified block diagram of an example of an arithmetic operation circuit shown in Fig. 3.

Fig. 5 is a characteristic graph for explaining an operation of the arithmetic operation circuit shown in Fig. 4.

20 Fig. 6 is a simplified circuit block diagram of another example of the arithmetic operation circuit shown in Fig. 3.

Fig. 7 is a characteristic graph for explaining the operation of the arithmetic operation circuit shown in Fig. 6.

Fig. 8 is a simplified circuit block diagram of still another example of the arithmetic operation circuit shown in Fig. 3.

30 Figs. 9 (a) to 9 (e) are waveform charts for explaining the operation of the arithmetic circuit shown in Fig. 8.

Fig. 10 is a characteristic graph for explaining the operation of the arithmetic circuit shown in Fig. 8.

35 Fig. 11 is a simplified circuit block diagram

of further example of the arithmetic operation circuit shown in Fig. 3.

Figs. 12 (a) to 12 (f) are waveform charts for explaining the operation of the circuit shown in Fig.

5 11.

Fig. 13 is a simplified circuit block diagram of a level limit processing block shown in Fig. 11.

Fig. 14 is a simplified circuit block diagram of a delay correction processing block shown in Fig. 11.

10 Fig. 15 is a simplified circuit block diagram of an LPF (Low Pass Filter) data processing block shown in Fig. 11.

Fig. 16 is a simplified circuit block diagram of a filter characteristic approximation processing
15 block shown in Fig. 11.

Fig. 17 is a simplified circuit block diagram of a level detection processing block shown in Fig. 11.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Reference will hereinafter be made to the
20 drawings in order to facilitate understanding of the present invention.

Fig. 2 shows a preferred embodiment of a video digital signal processing circuit for processing an image signal (input video signal) derived from a video
25 camera.

As shown in Fig. 2, the digital signal processing circuit 1 includes three series-connected signal processing blocks 5, 6 and 7, disposed between a data input terminal 2 to which an input video signal
30 (D_{in}) is supplied and data output terminal 8 from which the processed video signal (D_{out}) is outputted, for carrying out predetermined signal processings for the input digital signal (D_{in}) such as white balance adjustment, gamma correction, level clip, image
35 enhancement, and so on.

An input data switching circuit 4 is installed

between the data input terminal 2 and signal processing block 5 for switching and connecting either the data input terminal 2 or operation control data output terminal 31 of the control block 3 to the signal processing block 5. These input data switching circuits 4 and signal processing blocks 5, 6, and 7 receive a blanking signal (BK) indicating whether the input digital signal (D_{in}) is at a blanking interval via a blanking signal output terminal 33 of the control block 3.

Furthermore, the above-described signal processing block 7 supplies the output digital signal (D_{out}) to the above-described data output terminal 8 and to the control block 3. In addition, an external circuit (not shown in Fig. 2) is connected to the control block 3 for transmitting and receiving various data to and from the control block 3.

The above-described input data switching circuit 4 connects the control block 3 to the signal processing block 5 in response to the blanking signal (BK) supplied from the control block 3 when the input digital signal (D_{in}) is at the blanking interval. The above-described control block 3 adds operation control data (CD) of the respective signal processing blocks 5, 6, and 7 into the blanking interval of the input digital signal (D_{in}).

The operation control data (CD) includes block specification data for specifying any one of the signal processing blocks 5, 6, and 7 and operation specifying data instructing the specified signal processing block to operate. The above-described respective signal processing blocks 5, 6, and 7 read the block specifying data of the operation control data (CD) in response to the blanking signal (BK) supplied from the control block 3. When they are specified by means of the block specifying data, they read the operation instruction

data and carry out the predetermined signal processing instructed by means of the operation instruction data for the digital signal (D_{in}) to be supplied to the corresponding signal processing block thereafter.

5 Furthermore, in Fig. 2, the control block 3 determines whether the actual signal processing operation is normally carried out from the output digital signal (D_{out}) supplied from the above-described signal processing block 7.

10 Fig. 3 shows a specific construction of the signal processing block 5 shown in Fig. 2.

 In Fig. 3, the signal processing block 5 includes an input data switching circuit 52, an output data switching circuit 53, an arithmetic operation
15 circuit 54, and a control circuit 55. The input data switching circuit 52 is connected to a data input terminal 51 via which the input digital signal (D_{in}) is supplied. The output data switching circuit 53 is connected to the data input terminal 51 for supplying
20 the output digital signal (D_{out}) to the data output terminal 56. The arithmetic operation circuit 54 carries out the signal processing for the input digital signal (D_{in}) supplied via the input data switching circuit 52 and supplies the processed signal to the output digital
25 switching circuit 53. The control circuit 55 controls the operation of the arithmetic operation circuit 54 in accordance with the operation control data (CD) supplied via the input data switching circuit 52.

 The above-described control circuit 55
30 controls each switching operation according to the contents of the blanking signal (BK) supplied from the blanking signal output terminal 33 of the control block 3 via the blanking signal output terminal 57 such that during the video signal interval the above-described
35 input data switching circuit 52 connects the input data terminal 51 to the arithmetic operation circuit 54, the

output data switching circuit 53 connects the arithmetic operation circuit 54 to the data output terminal 56. The arithmetic operation circuit 54 then carries out the predetermined signal processing for the input digital signal (D_{in}) supplied via the input data terminal 51 and outputs the processed signal via the data output terminal 56.

In addition, the above-described control circuit 55 controls, in response to the blanking signal (BK), each switching operation such that during the blanking interval the input data switching circuit 52 connects the data input terminal 51 to the control circuit 55 and the output data switching circuit 53 connects the data input terminal 51 to the data output terminal 56. The input digital signal (D_{in}) supplied to the above-described data input terminal 51 is directly outputted via the data output terminal 56.

Furthermore, the control circuit 55 responsive to the blanking signal reads the block specifying data from the operation control data (CD) supplied from the control block 3 during the blanking interval. Then, the control circuit 55 further reads the operation instruction data when specified by the block specification data in the operation control data (CD) and controls the arithmetic operation circuit 54 such that the signal processing specified by the operation specification data is carried out for the input digital signal to be subsequently supplied thereto. Hence, the signal processing block 5 can carry out a desired signal processing for the input digital signal (D_{in}) according to the instruction of the operation control data (CD).

In addition, the control circuit 55 controls the above-described data switching circuit 53 in response to the instruction of the operation instruction data so that an additive data output terminal 58 is connected to the data output terminal 56. During the

blanking interval of the input digital signal (D_{in}), the data, e.g., indicating the present signal processing situation in the blockscan be outputted to the following stage.

5 It is noted that the other signal processing blocks 6 and 7 are also constructed substantially in the same way as the above-described signal processing block 5. The operation control data (CD) added into the input digital signal (D_{in}) is read during the blanking
10 interval so that the desired signal processing according to the operation control data (CD) is carried out for the input digital signal (D_{in}).

Hence, in the digital signal processing circuit 1, the above-described control block 3 can
15 control the signal processings of each signal processing block 5, 6, and 7 through the operation control data (CD) added into the blanking interval of the input digital signal (D_{in}). Since the signal line for inputting and outputting the input digital signal (D_{in})
20 can be used to input or output the above-described operation control data (CD), many signal lines can accordingly be omitted which inputs or outputs the above-described operation control data (CD) and have been connected respectively between the previously
25 proposed signal processing blocks. At the same time, great numbers of data can be inputted and outputted at high speeds. Hence, the digital signal processing circuit 1 can be achieved as a high-density and simply constructed digital signal processing circuit and can
30 carry out a more complex signal processing.

It is noted that the present invention is not limited only to the preferred embodiment shown in Figs. 2 and 3. The individual signal processing blocks may be constituted by three or more blocks and the operation
35 control data (CD) may be inputted from the above-described data output terminal 8 during the

blanking interval of the input digital signal (D_{in}) and supplied to the respective signal processing blocks 5, 6, and 7.

According to the present invention, the signal
5 lines for inputting and outputting the input digital
signal are used to input or output the operation control
data and the operation control data added to the
blanking interval of the input digital signal are used
to control the signal processing of the plurality of
10 signal processing blocks. Hence, since the digital signal
processing circuit according to the present invention
can input or output the operation control data using the
signal lines for inputting and outputting the input
digital signal, many signal lines through which the
15 operation control data connected to the respective
signal processing blocks can be inputted and outputted
can be omitted and a great amount of data can be
inputted and outputted at high speeds.

Next, specific examples of the arithmetic
20 operation circuit 54 shown in Fig. 3 will be described
below.

First, a gamma correction circuit will be
described as one of the example of the arithmetic
operation circuit 54 with reference to Figs. 4, 5, 6,
25 and 7.

Fig. 4 shows the block diagram of a gamma
correction circuit as the representative arithmetic
operation circuit 54.

The gamma correction circuit (arithmetic
30 operation circuit) 54, comprises an approximation data
output circuit 202 to which the input data (D_{in}) is
supplied from the data input terminal 201, a look-up
table memory 203 to which the input data (D_{in}) is
supplied from the above-described data input terminal
35 201, and an adder 204 which adds the approximation data
(D_a) outputted from the approximation data output

circuit 202 to the correction data (Db) outputted from the memory 203 and supplies the added output data (D_{out}) to the data output terminal 205.

The approximation data output circuit 202
5 outputs an approximation data (Da) having the approximation characteristic shown in a broken line to which a broken line (polyginal) approximation is carried out for a non-linear conversion characteristic of the output data (D_{out}) of the arithmetic operation circuit
10 54 shown in a solid line with respect to the input data (D_{in}) along a horizontal axis of Fig. 5.

In addition, in the above-described look-up table memory 203, a correction data (Db) expressed as $(Db) = (D_{out}) - (Da)$ is previously written into an address
15 specified by the above-described input data (D_{in}). The correction data (Db) is, as expressed above, a difference between the output data (D_{out}) of the digital signal processing block 5 and the approximation data (Da) with respect to the input data (D_{in}).

20 The correction data (Db) written in the specified address by the input data (D_{in}) supplied in the input data supplied into an address line of the memory 203 is outputted on the data line. In addition, the adder 204 generates the output data (D_{out}) expressed
25 by $(D_{out}) = (Da) + (Db)$ by adding the approximation data (Da) outputted from the approximation data output circuit 202 to the correction data (Db).

In details, the arithmetic circuit 54 carries out a predetermined non-linear processing by adding: (a)
30 the approximation data (Da) having the approximation characteristic approximate to the non-linear conversion characteristic outputted from the approximation data output circuit 202 with respect to the input data (D_{in}) supplied to the above-described data input terminal 201
35 and (b) the correction data (Db) indicative of the difference between the output data (D_{out}) having the

non-linear conversion characteristic read from the table
look-up table memory 203 and the approximation data
(Da). The non-linear output data (D_{out}), i.e., the gamma
corrected data is outputted via the output data output
5 terminal 205.

Hence, the arithmetic operation circuit 54 can
remarkably reduce the non-linear output data (D_{out}) as
compared with the case where the non-linear output data
(D_{out}) is all written in the memory 203 since the
10 correction data (Db) written into the memory 203 is a
data indicative of the difference between the non-linear
output data (D_{out}) and approximation data (Da).
Consequently, the circuit scale can be reduced and the
power consumption can accordingly be reduced.

15 Fig. 6 shows other approximation data output
circuit 222 and the table look-up memory 223 in which
the approximation data output circuit 222 outputs the
approximation data (Da) indicated by a broken line of
Fig. 7 to which a step approximation is carried out for
20 the non-linear conversion characteristic of the output
data (D_{out}) indicated by a solid line of Fig. 7 with
respect to the input data (D_{in}) along the horizontal
axis shown in Fig. 7 using the table look-up memory 223
in the same way as the above-described memory 203. In
25 this example, the correction data (Db), i.e., the data
indicative of the difference between the output data
(D_{out}) having the non-linear conversion characteristic
with respect to the input data (D_{in}) and approximation
data (Da) of the step approximation characteristic
30 expressed as follows: $(Db) = (D_{out}) - (Da)$ is written
into the address specified by the input data (D_{in}).
Therefore, the predetermined non-linear processing is
carried out for the input data (D_{in}) supplied to the
data input terminal 201 so that the non-linear output
35 data (D_{out}) can be outputted from the data output
terminal 205. It is noted that the other circuit

cinstructions are the same as those in the above-described arithmetic operation circuit 54. The same reference numerals as those shown in Figs. 4 and 6 designate corresponding elements and their detailed explanations are omitted here.

Examples of the gamma correction circuits are shown in Figs. 4 and 6. In Figs. 4 and 6, the control of gamma characteristic is carried out by means of the control signal formed on the basis of the operation control data (CD) and the desired gamma characteristic is selected. Therefore, a plural kinds of table memories 203 in Fig. 4 or table memories 223 in Fig. 6 are prepared and a desired one of table memories is selected according to the control signal. Alternatively, the data in the memory table 203 or 223 may be transmitted as the control signal and this data may be written in the table memory 203 or 223 constituted by a RAM (Random Access Memory) so as to obtain a desired correction data (Db).

As another example of the arithmetic operation circuit 54, the construction of an aperture correction circuit, to which a level compensation circuit such as a knee circuit is connected as the successive stage thereof will be described below with reference to Fig. 8.

Each digital input video signal of three primary colors R(Red), G(Green), and B(Blue) is supplied to the arithmetic operation circuit 54. The three primary color video signals correspond to the data input (D_{in}) of Fig.3.

The video signal processing circuit in Fig. 8 includes the aperture correction circuit 310 for carrying out a aperture correction for each input video signals (R), (G), and (B) supplied to a corresponding input terminal 301R, 301G, and 301B, the level compensation processing circuit 330 for carrying out the level compression processing for each video signal for

which the aperture correction is carried out in the aperture correction circuit 310 and outputting the corrected video signal to each output terminal 302R, 302G, and 302B, and a control block 340 for variably
5 controlling a aperture correction quantity derived by the above-described aperture correction circuit 310. The control signal such that the level compression characteristic of the level compression processing circuit 330 is controlled according to the level of the
10 input video signal is supplied via a control input terminal 304 to the level compression processing circuit 330 and to the control block 340.

The above-described aperture correction circuit 310 includes: (a) a aperture correction signal
15 generation block 320 for selecting the aperture correction signal from the input video signal (G) supplied to the input terminal 301G; (b) three delay circuits 311R, 311G, and 311B for providing delay quantities corresponding to the processing durations
20 during which the signals are processed in the aperture correction signal generation blocks 320 for the respective input video signals (R), (G) and (B) on the respective input terminals 301R, 301 G, and 301B; and
(c) three adders 312R, 312G, and 312G for adding the
25 aperture correction signal supplied from the aperture correction signal generating block 320 to each video signal supplied via the three delay circuits 311R, 311G, and 311B.

The aperture correction signal generating
30 block 320 includes an aperture detection circuit 321 for detecting an aperture part of the input video signal (G) supplied to the above-described input terminal 301G, a level adder 322 for generating a predetermined output signal according to the level of the input video signal
35 (G) supplied to the input terminal 301G, a multiplier 323 for multiplying the output signal of the aperture

detection circuit 321 by the output signal of the level adder 322, and a noise elimination circuit 324 for eliminating noise components from the output signal of the multiplier 323.

5 The aperture detection circuit 321 generates an output signal as equivalently shown in Fig. 9 (b) upon detection of a rising edge and falling edge of a waveform indicative of the aperture part of the input video signal (G) equivalently shown in Fig. 9 (a)
10 received from the input terminal 301G.

 The output signal of the aperture detection circuit 321 is supplied to the multiplier 323 and multiplied by the signal of the level adder 322 outputted according to the level of the input video
15 signal (G) supplied to the input terminal 301G so as to be subjected to a so-called level-dependent processing and is formed in a signal waveform as equivalently shown in Fig. 9 (c). Thereafter, the output signal described
20 above is supplied to the above-described noise elimination circuit 324. It is noted that the output signal of the above-described level adder 322 defines the aperture correction quantity of the aperture
25 correction processing carried out for the respective input video signals (R), (G), and (B) in the aperture correction circuit 310 and is generated in the non-linear form according to the level of the input
30 video signal (G) so as to carry out a favorable aperture correction processing. The noise elimination circuit 324 carries out a so-called crisping in which minute level signals included in the output signal of the multiplier
323 is eliminated as the noise components and generates the aperture correction signal equivalently shown in Fig. 9(d).

 Each adder 312R, 312G, and 312B in the
35 aperture correction circuit 310 carries out the addition processing for the aperture correction signal supplied

from the aperture correction signal generating block 320 and each input video signal (R), (G), and (B) supplied via the corresponding delay circuits 311R, 311G, and 311B and the video signals thus subjected to the aperture correction are supplied to the above-described level compression processing circuit 330. That is to say, for example, in one of the adders 312G, the aperture correction signal supplied from the aperture correction signal generating block 320 is added to the input video signal (G) so that an overshooting or undershooting waveform which has placed emphasis on the aperture part is added to the rising edge or falling edge of the waveform of the input video signal. Thus, the aperture compensated video signal as shown in Fig. 9 (e) is produced.

It is noted that although delay times inherently generated during their signal processings are not taken into consideration for the signal waveforms shown in Figs. 9 (a) to 9 (e), each delay circuit 311R, 311G, and 311B in the aperture correction circuit 310 compensates for the time errors described above so that the timing at which each input video signal (R), (G), and (B) appears coincides with that at which the aperture correction signal appears.

The above-described level compression processing circuit 330 carries out the level compression processing for each video signal (R), (G) and (B) which has been subjected to the aperture correction and has been supplied from the aperture correction circuit 310. The level compression circuits 331R, 331G, and 331B constitute the level compression processing circuit 330, each of which outputting the processed video signal to the corresponding output terminal 302R, 302G, and 302B. The control signal is supplied to the respective level compression circuits 331R, 331G, and 331B via the input terminal 304.

Each level compression circuit 331R, 331G, and 331B carries out a so-called knee correction etc. by carrying out the level compression processing for the non-linear characteristic set selectively according to the control signal from the plurality of non-linear characteristics such as the level characteristics of the output signal along the vertical axis with respect to the level of the input signal along the horizontal axis, as shown in Fig. 10.

It is noted that the level compression characteristic is used to change the level of the video signal and may describe a smoothly increasing curve or may describe a concave-shaped secondary degree curve.

The control block 340 comprises a first control circuit 341 for controlling the level adder 322 and a second control circuit 342 for controlling the noise elimination circuit 324. These first and second control circuits 341, 342 receive the control signal via the input terminal 304.

The first control circuit 341 controls the input-and-output characteristic of the level adder 322 so that the output video signal does not provide an unnatural image through the level compression processing carried out through the level compression processing circuit 330, thus variably controlling a quantity of the aperture correction provided in the aperture correction circuit 310 for each input video signal (R), (G), and (B).

In addition, the second control circuit 342 changes the noise elimination characteristic of the noise elimination circuit 324 so that the noise is not increased in the output video signal through the level compression processing carried out by means of the level compression processing circuit 330, thus controlling in such a way that the minute level signal components of the aperture signal are eliminated to a predetermined

amount.

In the way described above, the video signal processing apparatus in the example described above, the aperture correction quantity of the above-described aperture correction circuit 310 is variably controlled, interlocking with the setting characteristic of the level compression processing circuit 330. Therefore, a favorable aperture correction processing can be achieved together with the level compression processing according to the levels of the input video signals (R), (G), and (B).

It is noted that the level adder 322, noise elimination circuit 324, and each level compression circuit 331R, 331G, and 331B can non-linearly control each corresponding characteristic by controlling the write and read of data, e.g., in the look-up table constituted by the memory.

In the preferred embodiment described above, when the input video signal is supplied, the aperture correction circuit carries out the aperture correction processing for the input video signal, the level compression processing circuit carries out the level compression processing for the video signal subjected to the aperture correction processing to generate the output video signal. Then, the control circuit variably controls the quantity of the aperture correction derived from the aperture correction circuit, interlocking with the set characteristic of the level compression processing circuit.

Consequently, since, in the video signal processing apparatus according to the preferred embodiment described above, the quantity of the aperture correction added to the input video signal is variably controlled in association with the set characteristic of the level compression processing circuit, a favorable aperture correction processing can be carried out

according to the level of the input video signal together with the level compression processing.

5 An example of a digital clip circuit which digitally carries out so-called white clip, dark clip, and so on will be described below with reference to Figs. 11 to 17 as a last example of the arithmetic operation circuit 54 shown in Fig. 3.

10 In Fig. 11, an input data (D_{in}) is supplied via a data input terminal 402 to a digital clip circuit 401 and an upper limit data (D_h) is supplied to the digital clip circuit 401 via an upper limit data input terminal 403. In addition, a lower limit data (D_l) is supplied to a level limit processing block 410 via a lower limit data input terminal 404.

15 The output data (D_1) of the level limit processing block 410 is supplied to a delay correction processing block 420 and to a low-pass filter (LPF) data processing block and a filter characteristic approximation processing block 440. The output data (D_4) of the above-described filter characteristic approximation processing block 440 is supplied to the level detection processing block 450. Together with the upper limit data (D_h) supplied via the upper limit data input terminal 403, the lower limit data (D_l) is supplied via the lower limit data input terminal 404. A synthesizing processing block 460 receives the output data (D_2) of the delay correction processing block 420, the output data (D_3) of the above-described LPF data processing block 430, and the output data (D_5) of the level detection processing block 450. An output data (D_{out}) of the synthesizing processing block 460 is supplied to a data output terminal 405.

35 Series-connected circuits comprising a digital-to-analog (D/A) converter 406 and an interpolation filter 407 are connected to a data output terminal 405 of the digital clip circuit 401 directly or

via another digital signal processing circuit. Then, an output data (D_{out}) supplied to the data output terminal is converted by means of the digital-to-analog converter 406 and interpolation filter 407 and supplied to the analog signal output terminal 408.

The construction of each block constituting the digital clip circuit 401 will be described below with reference to Figs. 13 to 17. A specific signal processing will also be described with reference to a waveform chart equivalently showing each data at parts of the digital clip circuit 401 shown in Fig. 12 in an analog form.

The above-described level limit processing block 410 comprises first and second switching circuits 412, 413 connected in series between the data input terminal 402 and data output terminal 411 and first and second comparators 414, 415 outputting the control signal for switching operations of the switching circuits 412, 413, respectively.

The first comparator 414 has one input terminal connected to the data input terminal 402, the other input terminal connected to the upper limit input terminal 403, and an output terminal connected to a control input end of the above-described first switching circuit 412. The second comparator 415 has one input end connected to the data input terminal 402, the other input end connected to the lower limit data input terminal 404, and an output end thereof connected to a control input end of the second switching circuit 413. The first switching circuit 412 has an output terminal switched between the data input terminal 402 and upper limit data input terminal 403.

The second switching circuit 413 is switched to connect both the output end of the first switching circuit 412 and lower limit data input terminal 404 to the data output terminal 411.

The first comparator 414 controls the switching connection of the first switching circuit 412 using the output signal therefrom as follows. In details, the first comparator 414 connects the data input terminal 402 to the second switching circuit 413 when the input data (D_{in}) supplied from the data input terminal 402 is smaller than the upper limit data (D_h) from the upper limit data input terminal 403. When the input data (D_{in}) is larger than the upper limit data (D_h), the above-described upper limit data input terminal 403 and second switching circuit 413 are connected. On the other hand, the second comparator 415 outputs the signal to control the switching connection of the second switching circuit 413 as follows. That is to say, the second comparator 415 connects the first switching circuit 412 to the above-described data output terminal 411 when the input data (D_{in}) supplied from the lower limit data input terminal 402 is larger than the lower limit data (D_l) supplied from the lower limit data input terminal 404. When the input data (D_{in}) is smaller than the lower limit data (D_l), the second comparator 415 connects the lower limit data input terminal 404 to the data output terminal 411.

Hence, the level limit processing block 410 connects the data input terminal 402 and data output terminal 411 via the first and second switching circuits 412, 413 so that the input data (D_{in}) is directly outputted from the data output terminal 411 if the input data (D_{in}) supplied via the data input terminal 402 is the data whose value is between the upper limit data (D_h) and lower limit data (D_l). In addition, when the input data (D_{in}) is the data above the upper limit data (D_h), the first switching circuit 412 connects the upper limit data input terminal data input terminal 403 to the input end of the second switching circuit 413. The upper limit data (D_h) is outputted from the data output

terminal 411 via the second switching circuit 413.

Furthermore, if the input data (D_{in}) is the data whose value is lower than the lower limit data (D_L), the second switching circuit 413 connects the lower limit data input terminal 404 to the data output terminal 411 so that the lower limit data (D_L) is outputted via the data output terminal 411.

In other words, the level limit processing block 410 carries out the level limit processing (so-called clip) such as to replace the data whose signal level is larger than the upper limit data (D_h) with the upper limit data (D_h) and replace the data whose signal level is smaller than the lower limit data (D_L) with the lower limit data (D_L).

For example, when in the level limit processing block 410 the data signal input terminal 402 of the digital clip circuit 401 receives the input data (D_{in}) shown in Fig. 12 (a), the digital clip circuit 401 carries out the level limit processing (so-called clip operation) according to the upper limit level indicated by the upper limit data (D_h) supplied to the upper limit data input terminal 403 and the lower limit level indicated by the lower limit data (D_L) supplied to the lower limit data input terminal 404. Thus, the level limit processing block 410 generates a data (D_1) shown in Fig. 12(b).

It is noted that the data (D_1) outputted from the data output terminal 411 of the level limit processing block 410 is supplied to a delay correction processing block 420, low-pass filter (LPF) data processing block 430, and filter characteristic approximation processing block 440.

The delay correction processing block 420 includes a delay circuit 422, as shown in Fig. 14. A data (D_2) is generated, as shown in Fig. 12(c), which provides a delay corresponding to one clock for the data

(D1) supplied to the data input terminal 421. The delay data (D2) is supplied to the data output terminal 423.

5 The reason for the generation of the delay data (D2) which is delayed by one clock with respect to the data (D1) supplied to the data input terminal 421 is to synchronize the data (D2) to be processed in the synthesizing processing block 460 with the timings of the data (D3) and data (D5).

10 The above-described data (D2) is converted into an analog signal via the digital-to-analog converter 406 and is converted into an analog output signal (S_{out}) through the interpolation filter 407. At this time, an overshooting occurs on the rising edge of the analog signal waveform as in the previously proposed
15 digital clip circuit so that the output waveform such as to exceed the upper limit level of the upper limit data (Dh).

20 The LPF data processing block 430 includes two delay circuits 432, 433 as shown in Fig. 15, adder 434, 1/2 multiplier, adder 436, and 1/2 multiplier 437, these circuits being connected in series between the data input terminal 431 and the data output terminal 438. The above-described delay circuits 432, 433 are circuits for delaying the data supplied to the corresponding input
25 end by one clock in the same way as delay circuit 422 described above. The adder 434 is a circuit for outputting addition data between the data outputted from the delay circuit 433 and the data (D1) supplied from the level limit processing block 410 to the data
30 input terminal 431. In addition, the subsequent adder 436 is a circuit for outputting the added data between the data derived from the 1/2 multiplier 435 and data derived from the delay circuit 432. The 1/2 multipliers 435, 437 outputs data of 1/2 the data supplied thereto,
35 respectively.

 The LPF data processing block 430 shown in

Fig. 15 generates data (D3). That is to say, suppose that the data outputted from the delay circuit 432 denotes a basic data $Z^0=1$, the data supplied to the data input terminal 431 from the level limit processing block 410 denotes a data Z^{-1} preceded by one clock, and the data outputted from the delay circuit 433 is the data Z^{+1} delayed by one clock. Then, a low-pass filter characteristic (F(1)) expressed as follows--- $F(1)=(Z^{-1} + 2 + Z^{+1})/4$ ---Equation 1---is used to process the data (D1) supplied to the data input terminal 431 from the level limit processing block 410. The LPF data processing block 430 supplies the above-described data (D3) from the data output terminal 438 to the above-described synthesizing processing block 460.

The LPF data processing block 430 supplies the data (D3) from the data output terminal 438 to the above-described synthesizing processing block 460.

In other words, when the LPF data processing block 430 receives the data (D1) shown in Fig. 12 (b) at its data input terminal 431, the data (D3) being generated such that the rate of change in the data is gradual and the one-clock delay is provided, as shown in Fig. 12 (d).

The filter characteristic approximation processing block 440 includes two delay circuits 442, 443 installed between the data input terminal 441 and data output terminal 447, the adder 444, 1/16 multiplier, and a subtraction circuit 446, these circuits being connected in series, and 18/16 multiplier 448 for multiplying 18/16 for the data outputted from the delay circuit 442 and supplying the 18/16 multiplied data to the subtraction circuit 446.

The delay circuits 442, 443 are the circuits for delaying and outputting the data supplied to their data input ends by one clock in the same way as described in the respective delay circuits 422, 432,

433. The adder 444 generates the data (D4). That is to say, the adder 444 is a circuit for outputting the addition data between the data supplied from the delay circuit 443 and data (D1) supplied from the level limit processing block 410 to the data input terminal 441. In addition, the 1/16 multiplier is a circuit for outputting the data 1/16 of the data supplied from the adder 444. Furthermore, the subtraction circuit 446 is a circuit for subtracting the data supplied from the 18/16 multiplier 448 from the data supplied from the 1/16 multiplier 445.

Suppose that in the filter characteristic approximation processing block 440, the data outputted from the delay circuit 442 is a basic data $z^0 = 1$, the data (D1) supplied from the level limit processing block 410 to the data input terminal 441 is a data z^{-1} preceded by one clock, and the data outputted from the delay circuit 442 is a data z^{+1} delayed by one clock.

The filter characteristic of the above-described interpolation filter 407 is approximated using the characteristic (F(2)) shown in the following equation 2.

$$F(2) = (-z^{-1} + 18 - z^{+1}) / 16 \text{ ---Equation 2}$$

The filter approximation characteristic (F(2)) is provided for the data (D1) supplied to the data input terminal 441 from the level limit processing block 410. The filter characteristic approximation processing block 440 supplies the data (D4) from the data output terminal 447 to the level detection processing block 450.

In other words, in the filter characteristic approximation processing block 440, the data (D4) shown in Fig. 12 (e) is outputted from the data output terminal 447 when the data (d1) shown in Fig. 12 (b) is supplied. The data (D4) indicates an approximation data, predicting a signal level of the analog output signal waveform in cases where the data (D2) is directly

converted into an analog output signal via the digital-to-analog (D/A) converter 406 and interpolation filter 407.

The above-described level detection processing block 450, as shown in Fig.17, includes a subtraction circuit 452 for subtracting the upper limit data (Dh) supplied to the upper limit data input terminal 403 from the data (D4) supplied to the data input terminal 451 from the filter characteristic approximation processing block 440 and a switching circuit 453 having one input end for receiving the output data (D+) of the subtraction circuit 452, the other input end for receiving the basic data [0], and the output end being connected to an adder 454. The switching circuit 453 has a control input end for receiving the control signal outputted from the output end of a comparator 456. The comparator 456 has one input terminal receiving the output data (D+) of the subtraction circuit 452 and the other input terminal receiving the basic data [0], whereby the comparator 456 controls the switching operation of the switching circuit 453. In addition, the output data (D-) of the subtraction circuit 457 for subtracting the data (D4) supplied to the data input terminal 451 from the lower limit data (Dl) supplied to the lower limit data input terminal 404 is supplied to one input end of a switching circuit 458. The other input end of the switching circuit 458 receives the basic data [0] and the output end thereof is connected to the adder 454. The switching operation of the switching circuit 458 is controlled by means of the control signal outputted from the output end of the comparator 459. The comparator 459 has one input end receiving the output data (D-) and the other input end receiving the basic data [0]. The adder 454 adds the data supplied from the output end of each switching circuit 454, 458 to generate the data (D5), the data

(D5) being supplied to the data output terminal 455.

The comparator 456 compares the data (D+) outputted from the subtraction circuit 452, i.e., the data (D+) subtracting the upper limit data (Dh) from the data (D4) supplied to the data input terminal 451 with the basic data [0]. When the data (D+) is larger than the basic data [0], the switching circuit 453 is controlled so that the subtraction circuit 452 is connected with the adder 453.

In addition, the comparator 456 controls the switching circuit 453 so that the basic data [0] is supplied to the adder 454 when the data (D+) is smaller than the basic data [0].

The comparator 459 compares the data (D-), which is a subtraction of the data (D4) supplied from the filter characteristic approximation processing block 440 to the data input terminal 451 from the lower limit data (Dl), i.e., the output data of the subtraction circuit 457, with the basic data [0]. When the data (D-) is larger than the basic data [0], the switching circuit 458 is controlled so that the subtraction circuit 457 is connected to the adder 454. In addition, when the above-described data (D-) is smaller than the basic data [0], the switching circuit 458 is controlled so that the basic data [0] is supplied to the adder 454. The data outputted from the switching circuits 453, 458 is added by means of the adder 454 and supplied to the data output terminal 455.

In details, the level detection processing block 450 outputs the basic data [0] from the data output terminal 455 when the data (D4) supplied from the filter characteristic approximation processing block 440 to the data input terminal 451 is a data whose value is intermediate between the upper limit data (Dh) and lower limit data (Dl). When the data (D4) has a value not between the upper and low limit data (Dh, Dl), a data

(D5) indicating a quantity by which the data level exceeds either of the data level (level-over quantity) is outputted from the output terminal 455. Hence, the above-described level detection processing block 450
5 generates the data (D5) indicated in Fig. 12 (f) corresponding to the level-over quantity of the data below the lower limit data (D_L) or above the upper limit data (D_H). The data (D5) is supplied from the output data output terminal 455 to the synthesizing processing
10 block 460.

The synthesizing processing block 460 receives each data (D2), (D3), and (D5) and includes (as shown in Fig. 11) three multipliers 461, 463, 464, a subtraction circuit 462, and the adder 465. The multiplier circuit
15 461 outputs the data (D6) which is a multiplication of the data (D5) supplied from the level detection processing block 450 by a predetermined constant [A]. The subtraction circuit 463 outputs the data (D7) outputted from the subtraction circuit 462 and the data
20 (D8) of the data (D7) outputted from the subtraction circuit 462 and multiplied by the data (D2) supplied from the delay correction processing block 420. The multiplier 464 outputs the data (D9) which is a multiplication of the data (D6) outputted from the
25 multiplier 461 and data (D3) outputted from the LPF data processing block 430.

The adder 465 provides the data (Dout), an addition of the data (D9) outputted from the multiplier 464 to the data (D8) outputted from the multiplier 463,
30 for the data output terminal 405.

In the way described above, the above-described synthesizing processing block 460 provides the characteristic ($F(3)$) shown in an equation 3 for the data (D2) supplied from the delay correction circuit 420 to generate the output data (Dout) at the
35 data output terminal 405.

The equation 3 is expressed as follows:

$$\begin{aligned} F(3) &= \alpha (1/2 + (z^{-1} + z^{+1})/4) + (1-\alpha) \\ &= 1 + ((z^{-1} + z^{+1})/4 - 1/2) \alpha \\ &\text{---Equation 3} \end{aligned}$$

5 In the equation 3, α denotes a value of the data (D5) outputted from the level detection processing block 450 and multiplied by the constant [A] of the multiplier 461.

 In more details, in the synthesizing
10 processing block 460, the multiplier 464 generates the correction data (D9) which is a multiplication of the data (D6) changing according to the data (D5) outputted from the level detection processing block 450 by the data (D3) supplied from the LPF data processing block
15 430 for which the low-pass filter characteristic is provided.

 Then, in the synthesizing processing block 460, the adder 465 adds the correction data (D9) to the data (D2) supplied from the level limit processing block
20 410 via the delay correction processing block 420 for which the level limit is provided and the added data is outputted as the output data (D_{out}).

 Hence, when the data (D2) indicated in Fig. 12 (c), data (D3) indicated in Fig. 12(d), and data (D5)
25 indicated in Fig. 12 (f) are supplied to the synthesizing processing block 460, the multiplier 461 generates a data (D6) shown in Fig. 12(g) by multiplying the data (D5) supplied to the level detection processing block 450 by the predetermined constant [A]. The data
30 (D6) is supplied to the subtraction circuit 462 and multiplier 464, respectively. The data (D6) corresponds to a variable [α] indicated in the equation 3 and is varied according to the value of the data (D5).

 The subtraction circuit 462 generates a data
35 (D7) shown in Fig. 12 (h) by subtracting the data (D6) from the basic data [1] and supplies the data (D7) to

the multiplier 463. The multiplier 463 generates a data (D8) shown in Fig. 12 (i) by multiplying the data (D2) supplied from the delay correction processing block 420 by the data (D7) and supplies the data (D8) to the adder 465. The multiplier 464 generates the data (D9) shown in Fig. 12 (j) by multiplying the data (D6) supplied from the multiplier 461 by the data (D3) supplied from the LPF data processing block 430 and supplies the data (D9) to the adder 465. The adder 465 generates the output data (Dout) shown in Fig. 12 (k) by adding the data (D8) to the data (D9) and supplies the data (Dout) to the output terminal 405.

In this case, the output data (Dout) is such that the change rate of parts of the data (D2) corresponding to the upper limit data (D_h) and lower limit data (D_l) are slightly reduced according to an overshooting quantity generated when the data (D2) is converted into the analog form and is passed through the interpolation filter 407.

The output data (Dout) derived from the data output terminal 405 of the digital clip circuit 401 is converted into the analog output signal (S_{out}) shown in Fig. 12 (l) by means of the digital-to-analog (D/A) converter 406 and interpolation filter 407 and outputted via the signal output terminal 408, as shown in Fig. 11.

The analog output signal (S_{out}) has a waveform approximately equal to that equivalently shown in the analog signal form and the overshooting causes the analog output signal (S_{out}) not to exceed the upper limit level of the upper limit data (D_h).

In the way described above, the digital clip circuit 401 in the example shown in Fig. 11 generates the output data (Dout) by adding the correction data (D9) to the data (D2) in a case when the overshooting occurs during the passage of the analog data (D2) through the interpolation filter 407, the data (D2)

being generated by carrying out the level limit processing for the input data (D_{in}) through the level limit processing block 410. Thus, in the case where the input data (D_{in}) is formed of the analog signal and is
5 passed through the interpolation filter 407, the output data (D_{out}) can be generated such as to be converted into a favorable analog signal (S_{out}) without occurrence of overshooting.

The same processing is carried out for an
10 undershooting generated on a falling edge of a waveform of the analog output signal (S_{out}) in the digital clip circuit 401, although the explanation thereof is omitted here.

If the digital clip circuit 401 is used as the
15 arithmetic operation circuit 54 shown in Fig. 3, the upper limit data (D_h) and lower limit data (D_l) can be controlled in response to the control signal derived from the control circuit 55.

WHAT IS CLAIMED IS:

1. A digital signal processing circuit used in a video camera for processing a digital video signal having an effective signal interval and a blanking interval in a repeated fashion, said digital signal processing circuit comprising:
 - an input terminal supplied with the digital video signal;
 - control data generating means for generating a control data with a block address;
 - control data inserting means for inserting said control data with the block address into the blanking interval of said digital video signal; and
 - a plurality of signal processing circuit blocks connected in series with each other,each of said signal processing circuit blocks processing the digital video signal of the effective signal interval in accordance with the control data having the block address designating the corresponding block and each of said signal processing blocks including control data separating means for separating the control data having the block address designating the corresponding block.
2. A digital signal processing circuit according to claim 1, wherein each of said signal processing circuit blocks further includes an operating circuit supplied with the digital video signal and the control data for processing the digital video signal and the control data for processing the digital video signal effective signal interval in accordance with the control data and supplying the processed signal to the following block.
3. A digital signal processing circuit according to claim 2, wherein each of said processing circuit blocks includes a control circuit for decoding the block address and for controlling said separating means such

that the control data having the block address designating the corresponding block is separated and the control data having the block address designating other than the corresponding block is supplied to the following block.

5 4. A digital signal processing circuit according to claim 2, wherein said operating circuit of one of said signal processing blocks includes a gamma correction circuit for controlling the input-output characteristic of the digital video signal and said control data controls the input-output characteristics.

10 5. A digital signal processing circuit according to claim 4, wherein said gamma correction circuit includes a polygonal approximation data generating means, correcting data table having the data corresponding to the difference between the polygonal approximate data and the desired data and adder means for adding the polygonal approximate data and the data derived from the correcting data table, and said control data controls the output data of said correcting data table.

15 6. A digital data signal processing circuit according to claim 4, wherein said gamma correction circuit includes a step approximate data generating means, correcting data table having the data corresponding to the difference between the step approximate data and the desired data and adder means for adding the step approximate data and the data derived from the correcting data table, and said control data controls the output data of said correcting data table.

20 7. A digital signal processing circuit according to claim 2, wherein said operating circuit of one of said signal processings includes an aperture correction circuit having an aperture correction signal from the digital video signal and adder means for adding the

aperture correction signal to said digital video signal,
and a level compression circuit supplied with the output
of said aperture correction circuit, and said control
data controls the level of said aperture correction
5 signal and the characteristics of said level compression
circuit.

8. A digital signal processing circuit according
to claim 2, wherein said operating circuit of one of
said signal processing circuit blocks includes a white
10 clip circuit and a dark clip circuit, and said control
data controls the white clip level and the dark clip
level.

9. A digital signal processing circuit constructed
15 and arranged to operate substantially as hereinbefore
described with reference to and as illustrated in figures
2 to 17 of the accompanying drawings.